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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,614	03/31/2000	David W. Grawrock	042390.P8084	2176

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EXAMINER	
ZIA, SYED	

ART UNIT	PAPER NUMBER
2131	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/540,614	GRAWROCK, DAVID W.	
	Examiner	Art Unit	
	Syed Zia	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This office action is in response to arguments filed on March 01, 2004 (Paper 6). Original application contained Claims 1-23. Applicant did not add or cancel any Claim, and left unchanged Claims 1-23. Therefore, presently Claims 1-23 are pending for consideration.

Response to Arguments

Applicant's arguments filed on March 01, 2004 (Paper 6) have been fully considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-23 are rejected under 35 U.S.C. 102(v) as being anticipated by Ishac et al. U.S. Patent No. 5,812,861.

2. Regarding Claim 1 Ishac teach a method (Fig.1-4) comprising:

implementing an integrated circuit device within an electronic system, the integrated circuit device including an override disable pin (col.6 line 18 to col.7 line 14); and

preventing modification of a representation of a primary pass-phrase when the override disable pin is asserted, the primary pass-phrase permitting access to stored information within the electronic system (col.7 line 40 to col.9 line 20).

3. Regarding Claim 9 Ishac teach a method (Fig.1-4) comprising:

enabling access to stored information within an electronic system upon assertion of an override disable pin of an integrated circuit device (col.6 line 18 to col.7 line 14); and

disabling access to the stored information despite assertion of the override pin of the integrated circuit device when an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin (col.7 line 40 to col.9 line 20).

4. Regarding Claim 14 Ishac teach a method (Fig.1-4) comprising:

enabling placement of an electronic system into an administrator mode upon assertion of an override disable pin of an integrated circuit device (col.6 line 18 to col.7 line 14, and col.9 line 49 to line 65); and

disabling placement of the electronic system into the administrator mode despite assertion of the override pin of the integrated circuit device when an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin (col.7 line 40 to col.9 line 20).

5. Regarding Claim 18 Ishac teach an electronic system (Fig.1-4) comprising:

a bus, a processor coupled to the bus, a system memory coupled to the bus, and an integrated circuit device coupled to the bus, the integrated circuit device including a memory (col.3 line 34 to line 64);

an override pin to enable access to information stored within the memory upon assertion of the override pin (col.6 line 18 to col.7 line 14);

an override disable pin to disable access to the information stored within the memory despite the assertion of the override pin when the override disable pin is asserted prior to assertion of the override pin (col.7 line 40 to col.9 line 20).

5. Claims 2, 3, 5-8, 10, 11, 13, 15-17, 19-21, and 23 are rejected applied as above rejecting Claims 1, 9, 14, and 18. Furthermore, Ishac teach and describe a system and method for protecting confidential information stored within an electronic (Fig.1-4), wherein

the integrated circuit device comprises a package to form a packaged integrated circuit device (col.7 line 27 to line 54);

- preventing of the modification of the primary pass-phrase includes setting a control storage element within the integrated circuit device upon assertion of the override disable pin (col.11 line 10 to line 15); and

disabling modification of the primary pass-phrase when the control storage element is set (col.10 line 44 to col.11 line 9);

the integrated circuit device further includes an override pin which, when asserted, allows a stored representation of the primary pass-phrase to be modified (col.11 line 23 to line 40;

the setting of the control storage element includes setting a bit of at least one control register configured for permanent state retention over a plurality of power (col.7 line 15 to line 25);

- the preventing of the modification of the primary pass-phrase includes signaling a control application software initiating a request for modification of the pass-phrase that a user is denied access to the stored information of the integrated circuit device unless the primary pass-phrase is correctly entered (col.7 line 63 to col.8 line 62);

a primary pass-phrase that includes a hash value of the primary pass-phrase (col.8 line 39 to line 62);

control storage element includes at least one control register configured for permanent state retention over a plurality of power cycles (col.10 line 53 to line 67);

the integrated circuit further comprises a package to contain the memory from which the override pin and the override disable pin protrude (Fig.1-4);

the memory of the integrated circuit device is non-volatile memory (col.7 line 15 to line 25);

the integrated circuit device further includes a control storage (col.4 line 39 to line 49);

the integrated circuit device 2 further includes a microcode to determine whether the override disable pin has been 3 asserted prior to assertion of the override pin (col.4 line 50 to col.6 line 7).

6. Claims 4, 12, and 22 are rejected applied as above rejecting Claims 3, 11, and 21. Furthermore, Ishac teach and describe a system and method for protecting confidential information stored within an electronic, wherein

- the control storage element is set after placing the electronic system in an administration mode upon correctly inputting the primary pass-phase into the electronic system (col.6 line 18 to col.7 line 14, and col.9 line 49 to line 65);

- the control storage element of the integrated circuit device includes at least one control register configured for permanent state retention over a plurality of power cycles (col.10 line 53 to line 67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed Zia whose telephone number is 703-305-3881. The examiner can normally be reached on Monday - Friday 9:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 703-305-9648. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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August 08, 2004